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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,241	HASHEMI, EBRAHIM	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 41-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39 and 41-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-5,7,8,9,11,12,14-21,23-25,27-38,41,42,44-47 are rejected under 35 U.S.C. 102(a) as being anticipated by Solomon et al. (USPN 6151659A). As appears in claim 1, Solomon et al. discloses a plurality of storage devices, a storage controller coupled to said plurality of storage devices, wherein said storage controller is configured to store data in the form of stripes where each stripe includes a plurality of data blocks stored across said plurality of storage devices, wherein each stripe further includes a redundancy data block in column 3, lines 26-39.

Solomon et al. discloses wherein said storage controller is further configured to initialize a given stripe in response to receiving a write request to write a new data block at a particular location of said given strip and detecting a mismatch in block verification information associated with an existing data block at the particular location of said given stripe to be updated, wherein said storage controller is configured to initialize said given stripe by generating a corresponding redundancy data block for said given stripe based on at least the new data block to be written to said given stripe in column 6, line 64 – column 7, line 18. It is inherent for a RAID system to have a controller.

3. As per claim 2, Solomon et al. discloses said storage controller is configured to initialize said given stripe by reading one or more remaining data blocks of said given stripe and generating the corresponding redundancy data block for said given stripe based on the remaining data blocks and the new data block in column 6, line 64 – column 7, line 18.

4. As per claim 3, Solomon et al. discloses said redundancy data block contains parity data calculated from said other data blocks in column 2, lines 5-11.

5. As per claim 4, Solomon et al. discloses said block verification information associated with a particular data block includes a code dependent upon data contained within said particular data block in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

6. As per claim 5, Solomon et al. discloses said code is an error detection code in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

7. As per claim 7, Solomon et al. discloses said storage controller is configured to detect a mismatch in said block verification information by comparing a value contained in a field of said particular data block for storing said error detection code to a recomputed error detection code computed from data within said particular data block read form one of said storage devices in column 6, line 64 – column 7, line 18.

8. As per claim 8, Solomon et al. discloses said block verification information associated with a particular data block includes an address associated with said particular data block in column 6, line 64 – column 7, line 18.

9. As per claims 9 and 25, Solomon et al. discloses said address is a logical block address for each particular block. It is inherent for a RAID system to be accessed by using logical block addressing.

10. As per claim 11, Solomon et al. discloses said block verification information of said particular data block further includes a code dependent upon data contained within said particular data block in column 6, line 64 – column 7, line 18.

11. As per claim 12, Solomon et al. discloses said code is an error detection code in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

12. As per claim 14, Solomon et al. discloses said plurality of storage devices is a disk drive in Figure 1B.

13. As per claim 15, Solomon et al. discloses said block verification information includes a block ID in column 6, line 64 – column 7, line 18.

14. As per claim 16, Solomon et al. discloses said storage controller is configured to implement RAID 5 functionality column 6, lines 1-9.

15. As per claim 17, Solomon et al. discloses a plurality of storage devices, a storage controller coupled to said plurality of storage devices, wherein said storage controller is configured to store data in the form of stripes where each stripe includes a plurality of data blocks stored across said plurality of storage devices, wherein at least one of the plurality of data blocks is a redundancy data block in column 3, lines 26-39.

Solomon et al. discloses wherein said storage controller is further configured to initialize a given stripe in response to receiving a write request to write a new data block at a particular location of said given stripe and detecting a mismatch in block verification

information in each of at least two existing data blocks of said given stripe, wherein one of the two existing data blocks is at the particular location of said given stripe to be updated, wherein said storage controller is configured to initialize said given stripe by generating a corresponding redundancy data block for said given stripe based on at least the new data block to be written to said given stripe in column 6, line 64 – column 7, line 18. It is inherent for a RAID system to have a controller.

16. As per claim 18, Solomon et al. discloses said storage controller is configured to initialize said given stripe by reading one or more remaining data blocks of said given stripe and generating the corresponding redundancy data block for said given stripe based on the remaining data blocks and the new data block in column 6, line 64 – column 7, line 18.

17. As per claim 19, Solomon et al. discloses said redundancy data block contains parity data calculated from said other data blocks in column 2, lines 5-11.

18. As per claim 20, Solomon et al. discloses said block verification information associated with a particular data block includes a code dependent upon data contained within said particular data block in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

19. As per claim 21, Solomon et al. discloses said code is an error detection code in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

20. As per claim 23, Solomon et al. discloses said storage controller is configured to detect a mismatch in said block verification information by comparing a value contained in a field of said particular data block for storing said error detection code to a

recomputed error detection code computed from data within said particular data block read form one of said storage devices in column 6, line 64 – column 7, line 18.

21. As per claim 24, Solomon et al. discloses said block verification information associated with a particular data block includes an address associated with said particular data block in column 6, line 64 – column 7, line 18.

22. As appears in claim 27, Solomon et al. discloses a host, a data storage subsystem coupled to said host, a plurality of storage devices, a storage controller coupled to said plurality of storage devices wherein said storage controller is configured to store data in the form of stripes where each stripe includes a plurality of data blocks stored across said plurality of storage devices, wherein each stripe further includes a redundancy data block in column 3, lines 26-39.

Solomon et al. discloses wherein said storage controller is further configured to initialize a given stripe in response to receiving a write request to write a new data block at a particular location of said given stripe and detecting a mismatch in said block verification information associated with an existing data block at the particular location of said given stripe to be updated and wherein said storage controller is configured to initialize said given stripe by generating a corresponding redundancy data block for said given stripe based on at least the new data block to be written to said given stripe in column 6, line 64 – column 7, line 18. It is inherent for a RAID system to have a controller.

23. As per claim 28, Solomon et al. discloses said storage controller is configured to initialize said given stripe by reading one or more remaining data blocks of said given

stripe and generating the corresponding redundancy data block for said given stripe based on the remaining data blocks and the new updated data block in column 6, line 64 – column 7, line 18.

24. As per claim 29, Solomon et al. discloses said redundancy data block contains parity data calculated from said other data blocks in column 2, lines 5-11.

25. As per claim 30, Solomon et al. discloses said block verification information associated with a particular data block includes an error detection code in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

26. As per claim 31, Solomon et al. discloses said block verification information associated with a particular data block includes an address associated with said particular data block in column 6, line 64 – column 7, line 18.

27. As appears in claim 32, Solomon et al. discloses storing data in the form of stripes within a plurality of storage devices where each stripe includes a plurality of data blocks stored across said plurality of storage devices wherein each stripe further includes a redundancy data block in column 3, lines 26-39.

Solomon et al. discloses initializing a given stripe in response to receiving a write request to write a new data block at a particular location of said given stripe and detecting a mismatch in block verification information associated with an existing data block at the particular location of said given stripe comprises generating a corresponding redundancy data block for said given stripe based on at least the new data block to be written to said given stripe in column 6, line 64 – column 7, line 18.

28. As per claim 33, Solomon et al. discloses wherein said initializing said given stripe comprises reading one or more remaining data blocks of said given stripe and generating the corresponding redundancy data block for said given stripe based on the remaining data blocks and the new data block in column 6, line 64 – column 7, line 18.

29. As per claim 34, Solomon et al. discloses said redundancy data block contains parity data calculated from said other data blocks on page 4, paragraph 0032, "As is illustrated, data stripe 200 includes one parity sector 204 for each data sector in the stripe."

30. As per claim 35, Solomon et al. discloses said block verification information of a particular data block includes an error detection code in column 2, lines 5-11.

31. As per claim 36, Solomon et al. discloses said block verification information associated with said particular data block further includes an address associated with said particular data block in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

32. As per claim 37, Solomon et al. discloses said block verification information associated with said particular data block includes an address associated with said particular data block in column 6, line 64 – column 7, line 18 and column 6, lines 1-9.

33. As per claim 38, Solomon et al. discloses said detecting a mismatch in said block verification information comprises comparing a value contained in a field of said particular data block for storing said error detection code to a recomputed error detection code computed from data within said particular data block read form one of said storage devices in column 6, line 64 – column 7, line 18.

34. As per claim 41, Solomon et al. discloses wherein in response to receiving the write request said storage controller is configured to read the existing data block to determine whether a mismatch exists in the block verification information associated within the existing data block in column 6, line 64 – column 7, line 18.

35. As per claim 42, Solomon et al. discloses wherein said storage controller is configured to initialize said given stripe by generating the corresponding redundancy data block for said given stripe based on the new data block and a known data pattern to be written to said given stripe at memory locations corresponding to one or more remaining data blocks of said given stripe in column 6, line 64 – column 7, line 18.

36. As per claim 44, Solomon et al. discloses wherein block verification information is associated with each of the plurality of data blocks and the redundancy data block in column 6, line 64 – column 7, line 18.

37. As per claim 45, Solomon et al. discloses wherein said storage controller is configured to initialize one or more stripes in said data storage subsystem depending upon whether write requests are received that correspond to the one or more stripes and depending upon whether a mismatch is detected in the block verification information associated with each of the one or more stripes in column 6, line 64 – column 7, line 18.

38. As per claim 46, Solomon et al. discloses wherein said storage controller is configured to initialize a subset of said stripes in said data storage subsystem and subsequent to initializing the subset of said stripes, initializing one or more remaining stripes in said data storage subsystem in column 6, line 64 – column 7, line 18.

39. As per claim 47, Solomon et al. discloses storing data in the form of stripes where each stripe includes a plurality of data blocks stored across said plurality of storage devices in column 3, lines 26-39.

Solomon et al. discloses initializing a subset of said stripes in said data storage subsystem; performing a partial write to at least one of said stripes of said subset; and subsequent to performing the partial write to at least one of said stripes of said subset, initializing one or more remaining stripes in said data storage subsystem stripe in column 6, line 64 – column 7, line 18.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 10,26,39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al. in view of IBM. As per claims 10, 26, 39, Solomon et al. fails to explicitly state detecting a mismatch in said block verification information comprises comparing a value contained in a field of said particular data block for storing said address to an expected value of said address for said particular data block read from one of said storage devices.

IBM discloses on page 189, "The solution to this problem is to record the LBA within the sector of data when it is written to the device and check the LBA when the data is read form the device."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to detect a mismatch in said block verification information comprises comparing a value contained in a field of said particular data block for storing said address to an expected value of said address for said particular data block read from one of said storage devices. A person of ordinary skill in the art would have been motivated to have detect a mismatch in said block verification information comprises comparing a value contained in a field of said particular data block for storing said address to an expected value of said address for said particular data block read from one of said storage devices because there is a need to determine if the write data has been sent to the write logical block address. IBM discloses on page 189, "Direct Access Storage Devices (DASDs) have no capability for determining if they have sent the host system incorrect data for a given Logical Block Address (LBA)."

42. Claims 6,13,22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al. in view of Archibald, Jr. et al. (US Publication Number 20020169995A1). As per claims 6,22, Solomon et al. fails to explicitly state error detection code is a cyclic redundancy check code.

Archibald, Jr. et al. discloses this limitation on page 4, paragraph 0032, "The one or more DSS_{ds} values can be Longitudinal Redundancy Check (LRC) values, Cyclical Redundancy Check (CRC) values or Checksum Values."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have error detection code be cyclic redundancy check code. A person of ordinary skill in the art would have been motivated to have error detection code be cyclic redundancy check code because cyclic redundancy check code is a type of error detection code that is used for checking errors for data stored in memory. This is disclosed on page 2, paragraph 0011.

43. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon et al. in view of Matsumoto (USPN 5737745A). As per claim 43, Solomon et al. fails to explicitly state the known data pattern is a pattern of all zeros. The known pattern is going to be used with the new data block in order to generate the corresponding redundancy data block for the stripe.

Matsumoto et al. discloses this limitation in column 1, lines 53-66.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the known data pattern be a pattern of all zeros. A person of ordinary skill in the art would have been motivated to have the known data pattern be a pattern of all zeros because a pattern of all zeros represents that data has been entered for all sections of a memory device when a memory device has first been brought on-line. Considine et al. (USPN 6425053B1) discloses this in the abstract, "The command causes a small data block of all zeroes written tot eh disk to be duplicated so that the entire container space in each disk is effectively written to."

44. Applicant's arguments with respect to claims 1-39,41-47 have been considered but are moot in view of the new ground(s) of rejection. The addition of new limitations in

the independent claims disclosed above prompted a new reference to be found, Solomon et al., to reject the independent claims; therefore, the arguments disclosed in the RCE for Archibald, Jr. et al. are moot.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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